MOTOROLA
SEMICONDUCTOR TECHNICAL DATA

Order number: MC100ES6056
Rev 3, 5/2004

MC100ES6056

2.5V / 3.3V ECL/PECL/LVDS Dual Differential 2:1 Multiplexer

The MC100ES6056 is a dual, fully differential 2:1 multiplexer. The differential data path makes the device ideal for multiplexing low skew clock or other skew sensitive signals. Multiple V_{BB} pins are provided.

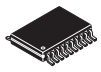
The V_{BB} pin, an internally generated voltage supply, is available to this device only. For single-ended input conditions, the unused differential input is connected to V_{BB} as a switching reference voltage. V_{BB} may also rebias AC coupled inputs. When used, decouple V_{BB} and V_{CC} via a 0.01 μF capacitor and limit current sourcing or sinking to 0.5 mA. When not used, V_{BB} should be left open.

The device features both individual and common select inputs to address both data path and random logic applications.

The 100ES Series contains temperature compensation.

Features

- 360 ps Typical Propagation Delays
- Maximum Frequency > 3 GHz Typical
- PECL Mode Operating Range: V_{CC} = 2.375 V to 3.8 V with V_{EE} = 0 V
- ECL Mode Operating Range: V_{CC} = 0 V with V_{EE} = -2.375 V to -3.8 V
- Open Input Default State
- Separate and Common Select
- Q Output Will Default LOW with Inputs Open or at V_{EE}
- V_{BB} Outputs
- LVDS Input Compatible



DT SUFFIX
20 LEAD TSSOP PACKAGE
CASE 948E



DW SUFFIX
20 LEAD SOIC PACKAGE
CASE 751D

ORDERING INFORMATION

Device	Package
MC100ES6056DT	TSSOP-20
MC100ES6056DTR2	TSSOP-20
MC100ES6056DW	SO-20
MC100ES6056DWR2	SO-20

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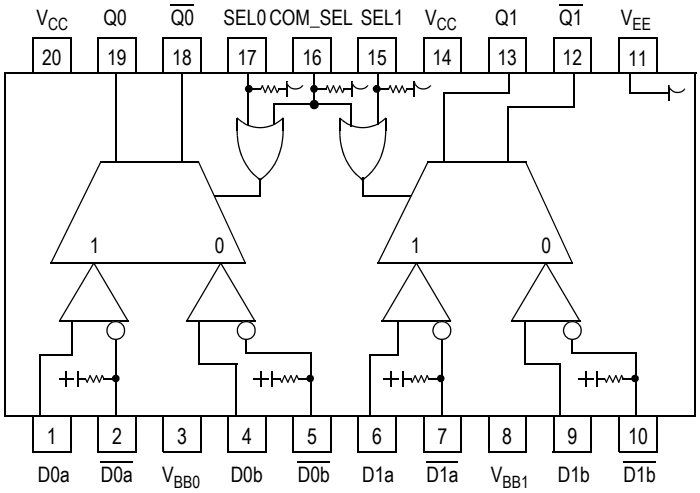

Warning: All V_{CC} and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.

Figure 1. 20-Lead Pinout (Top View) **and Logic Diagram**

* Input function will default LOW when left open.

Table 1. Pin Description

Pin	Function
D0a* – D1a*	ECL Input Data a
$\overline{D0a}$* – $\overline{D1a}$*	ECL Input Data a Invert
D0b* – D1b*	ECL Input Data b
$\overline{D0b}$* – $\overline{D1b}$*	ECL Input Data b Invert
SEL0* – SEL1*	ECL Indiv. Select Input
COM_SEL*	ECL Common Select Input
V_{BB0}, V_{BB1}	Output Reference Voltage
Q0 – Q1	ECL True Outputs
$\overline{Q0}$ – $\overline{Q1}$	ECL Inverted Outputs
V_{CC}	Positive Supply
V_{EE}	Negative Supply

Table 2. Function Table

SEL0	SEL1	COM_SEL	Q0, $\overline{Q0}$	Q1, $\overline{Q1}$
X	X	H	a	a
L	L	L	b	b
L	H	L	b	a
H	H	L	a	a
H	L	L	a	b

Table 3. General specifications

Characteristics		Value
Internal Input Pulldown Resistor		75 kΩ
Internal Input Pullup Resistor		75 kΩ
ESD Protection	Human Body Model Machine Model Charged Device Model	> 4 kV > 400 V > 2 kV
Thermal Resistance (Junction-to-Ambient)	0 LFPM, 20 TSSOP 500 LFPM, 20 TSSOP	140°C/W 100°C/W
	0 LFPM, 20 SOIC 500 LFPM, 20 SOIC	TBD TBD
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test		

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Table 4. Absolute Maximum Ratings[1]

Symbol	Characteristic	Conditions	Rating	Units
V_{SUPPLY}	Power Supply Voltage	Difference between V_{CC} & V_{EE}	3.9	V
V_{IN}	Input Voltage	$V_{CC} - V_{EE} \leq 3.6$ V	V_{CC} + 0.3 V_{EE} – 0.3	V
I_{OUT}	Output Current	Continuous Surge	50 100	mA mA
I_{BB}	V_{BB} Sink/Source Current		±0.5	°C
T_A	Operating Temperature Range		–40 to +85	°C
T_{STG}	Storage Temperature Range		–65 to +150	°C

1. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

Table 5. DC Characteristics (V_{CC} = 0 V, V_{EE} = –2.5 V±5% or 3.8 V to –3.135 V; V_{CC} = 2.5 V±5% or 3.135 V to 3.8 V, V_{EE} = 0 V)

Symbol	Characteristics	–40°C			0°C to 85°C			Unit
		Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		30	60		30	60	mA
V_{OH}	Output HIGH Voltage[1]	V_{CC}–1085	V_{CC}–960	V_{CC}–880	V_{CC}–1025	V_{CC}–930	V_{CC}–860	mV
V_{OL}	Output LOW Voltage[1]	V_{CC}–1950	V_{CC}–1695	V_{CC}–1500	V_{CC}–1950	V_{CC}–1705	V_{CC}–1500	mV
V_{IH}	Input HIGH Voltage	V_{CC}–1165		V_{CC}–880	V_{CC}–1165		V_{CC}–880	mV
V_{IL}	Input LOW Voltage	V_{CC}–1810		V_{CC}–1475	V_{CC}–1810		V_{CC}–1475	mV
V_{BB}	Output Reference Voltage	V_{CC}–1380	V_{CC}–1290	V_{CC}–1220	V_{CC}–1380	V_{CC}–1290	V_{CC}–1200	mV
V_{PP}	Differential Input Voltage[2]	0.15		1.3	0.15		1.3	V
V_{CMR}	Differential Cross Point Voltage[3]	V_{CC} –2.3		V_{CC}–0.8	V_{CC} –2.3		V_{CC}–0.8	V
I_{IH}	Input HIGH Current			150			150	µA
I_{IL}	Input LOW Current	0.5			0.5			µA

1. Output termination voltage V_{TT} = 0V for V_{CC} = 2.5V operation is supported but the power consumption of the device will increase.
2. V_{PP} (DC) is the minimum differential input voltage swing required to maintain device functionality.
3. V_{CMR} (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the V_{CMR} (DC) range and the input swing lies within the V_{PP} (DC) specification.

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Table 6. AC Characteristics (V_{CC} = 0 V; V_{EE} = –2.5 V ±5% or –3.8 V to –3.135 V; V_{CC} = 2.5 V ±5% or 3.135 V to 3.8 V; V_{EE} = 0 V)[1]

Symbol	Characteristics	–40°C to 85°C			Unit
		Min	Typ	Max	
f_{max}	Maximum Frequency		> 3		GHz
t_{PLH}, t_{PHL}	Propagation Delay to Output Differential D to Q, $\overline{Q}$ SEL to Q, $\overline{Q}$ COM_SEL to Q, Q	300 300 300	400 430 490	500 600 650	ps ps ps
t_{SKEW}	Skew Output-to-Output[2] Part-to-Part		10	50 200	ps ps
t_{JITTER}	Cycle-to-Cycle Jitter RMS (1σ)			1	ps
V_{PP}	Minimum Input Swing	200	800	1200	mV
V_{CMR}	Differential Cross Point Voltage	V_{CC}–2.1		V_{CC}–1.1	V
t_r / t_f	Output Rise/Fall Time (20%–80%)	70	120	230	ps

1. Measured using a 750 mV source, 50% duty cycle clock source. All loading with 50Ω to V_{CC}–2.0 V.
2. Skew is measured between outputs under identical transitions. Duty cycle skew is defined only for differential operation when the delays are measured from the cross point of the inputs to the cross point of the outputs.

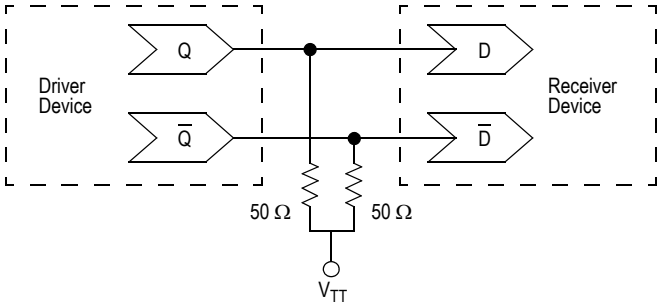

Figure 2. Typical Termination for Output Driver and Device Evaluation

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Marking Notes:

Device Nomenclature	20-Lead TSSOP Marking	20-Lead SOIC W/B Marking
MC100ES6056DT	6056	
MC100ES6056DW		MC100ES6056

Trace Code Identification for 20 SOIC: AWLYYWW

"A" – The First character indicates the Assembly location.
"WL" – The Second & Third characters indicate the Source Wafer Lot Tracking Code.
"YY" – The Fourth & Fifth characters indicate the Year device was assembled.
"WW" – The Sixth & Seventh characters indicate the Work Week device was assembled.

Trace Code Identification for 20 TSSOP: ALYW

"A" – The First character indicates the Assembly location.
"L" – The Second character indicates the Source Wafer Lot Tracking Code.
"Y" – The Third character indicates the "ALPHA CODE" of the year device was assembled.
"W" – The Fourth character indicates the "ALPHA CODE" of the Work Week device was assembled.

The "Y" Year ALPHA CODES

Year	Month	Work Week Code
A = 2003	FIRST 6 MONTHS	WW01 – WW26
B = 2003	SECOND 6 MONTHS	WW27 – WW52
C = 2004	FIRST 6 MONTHS	WW01 – WW26
D = 2004	SECOND 6 MONTHS	WW27 – WW52
E = 2005	FIRST 6 MONTHS	WW01 – WW26
F = 2005	SECOND 6 MONTHS	WW27 – WW52
G = 2006	FIRST 6 MONTHS	WW01 – WW26
H = 2006	SECOND 6 MONTHS	WW27 – WW52
I = 2007	FIRST 6 MONTHS	WW01 – WW26
J = 2007	SECOND 6 MONTHS	WW27 – WW52
K = 2008	FIRST 6 MONTHS	WW01 – WW26
L = 2008	SECOND 6 MONTHS	WW27 – WW52
M = 2009	FIRST 6 MONTHS	WW01 – WW26
N = 2009	SECOND 6 MONTHS	WW27 – WW52
O = 2010	FIRST 6 MONTHS	WW01 – WW26
P = 2010	SECOND 6 MONTHS	WW27 – WW52
Q = 2011	FIRST 6 MONTHS	WW01 – WW26
R = 2011	SECOND 6 MONTHS	WW27 – WW52
S = 2012	FIRST 6 MONTHS	WW01 – WW26
T = 2012	SECOND 6 MONTHS	WW27 – WW52
U = 2013	FIRST 6 MONTHS	WW01 – WW26
V = 2013	SECOND 6 MONTHS	WW27 – WW52
W = 2014	FIRST 6 MONTHS	WW01 – WW26
X = 2014	SECOND 6 MONTHS	WW27 – WW52
Y = 2015	FIRST 6 MONTHS	WW01 – WW26
Z = 2015	SECOND 6 MONTHS	WW27 – WW52

The "W" Work Week ALPHA CODES

1st 6 Months (WW01 – WW26)	2nd 6 Months (WW27 – WW52)
A = WW01	A = WW27
B = WW02	B = WW28
C = WW03	C = WW29
D = WW04	D = WW30
E = WW05	E = WW31
F = WW06	F = WW32
G = WW07	G = WW33
H = WW08	H = WW34
I = WW09	I = WW35
J = WW10	J = WW36
K = WW11	K = WW37
L = WW12	L = WW38
M = WW13	M = WW39
N = WW14	N = WW40
O = WW15	O = WW41
P = WW16	P = WW42
Q = WW17	Q = WW43
R = WW18	R = WW44
S = WW19	S = WW45
T = WW20	T = WW46
U = WW21	U = WW47
V = WW22	V = WW48
W = WW23	W = WW49
X = WW24	X = WW50
Y = WW25	Y = WW51
Z = WW26	Z = WW52

20 TSSOP Tracecode Marking Example:

5ABR

5 = Assembly Location

A = First Lot Assembled of this device in the designated Work Week

B = 2003 Second 6 Months, WW27 – WW52

R = WW44 of 2003

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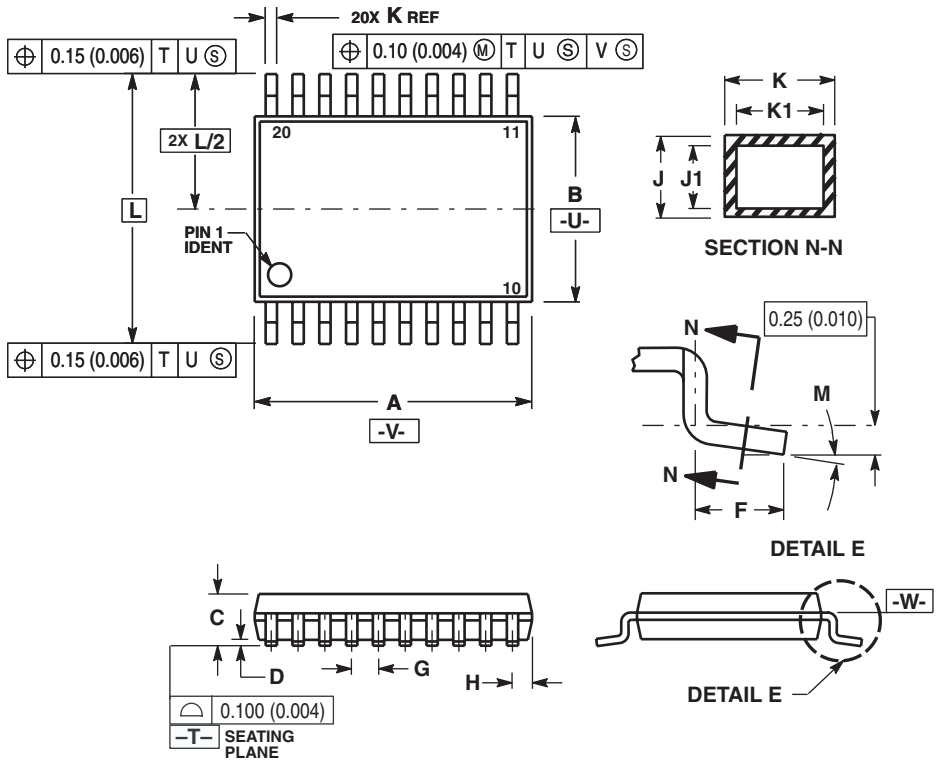
PACKAGE DIMENSIONS

DT SUFFIX
20 LEAD TSSOP PACKAGE
CASE 948E-02
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND BE ARE TO BE DETERMINED AT DATUM PLANE -W-.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	6.40	6.60	0.252	0.260
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.27	0.37	0.011	0.015
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

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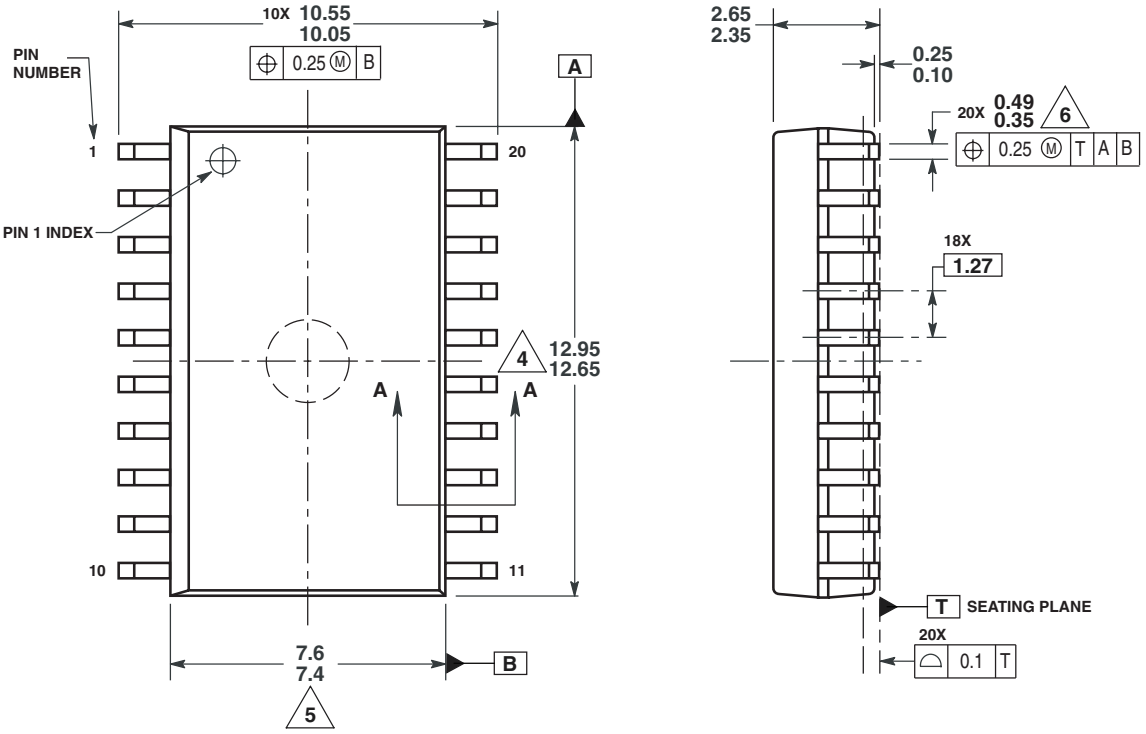
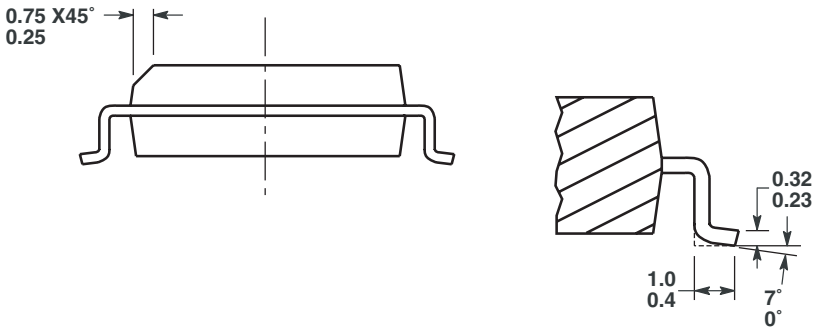
PACKAGE DIMENSIONS

DW SUFFIX
20 LEAD SOIC PACKAGE
CASE 751D-06
ISSUE H





SECTION A-A

NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
3. DATUMS A AND B TO BE DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
4. THIS DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS. MOLD FLASH, PROTRUSION OR GATE BURRS SHALL NOT EXCEED 0.15 MM PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
5. THIS DIMENSION DOES NOT INCLUDE INTER-LEAD FLASH OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED 0.25 MM PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
6. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE WIDTH TO EXCEED 0.62 MM.

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